IDEC Chip Design Contest

A -240dB-FOM and -115dBc/Hz-100kHz-PN, 7.7GHz-Ring-DCO-Based Digital PLL Using P/I-Gain Co-Optimization

KAIST EE
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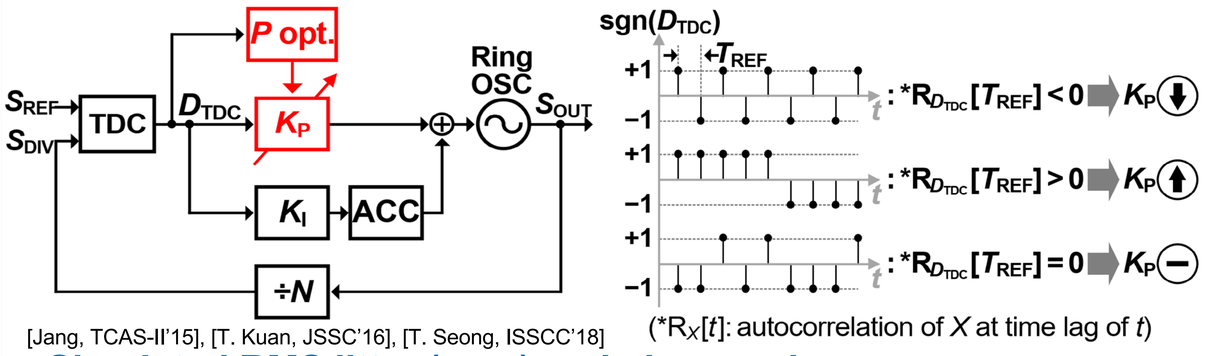
Integrated Circuits and Systems Lab

Introduction

■ **Conventional Ring-Oscillator-Based Digital PLLs**
– ***P*-path gain (K_P) optimization based on $R_{D_{TDC}}[T_{REF}]$**

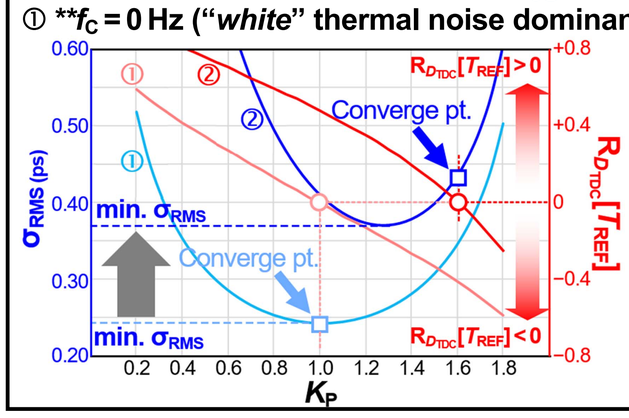


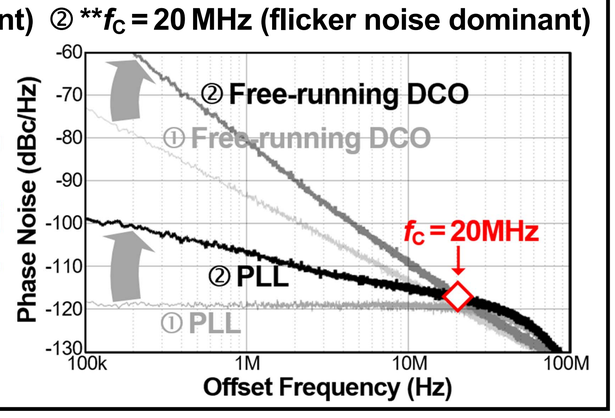
[Jang, TCAS-II'15], [T. Kuan, JSSC'16], [T. Seong, ISSCC'18]

(*$R_X[t]$: autocorrelation of X at time lag of t)

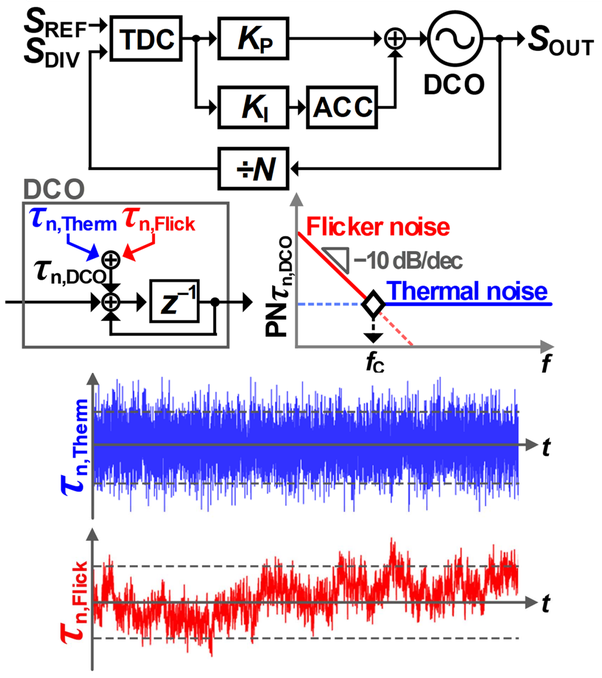
■ **Simulated RMS jitter (σ_{RMS}) and phase noise**
(f_{REF} = 125 MHz, N = 64, $K_I = 2^{-8}$, $PN_{Ring@100M}$ = −133dBc/Hz) (**f_C: flicker corner frequency)

① **f_C = 0 Hz ("*white*" thermal noise dominant) ② **f_C = 20 MHz (flicker noise dominant)



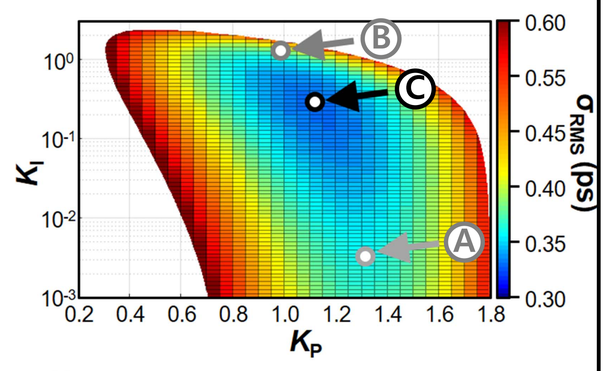


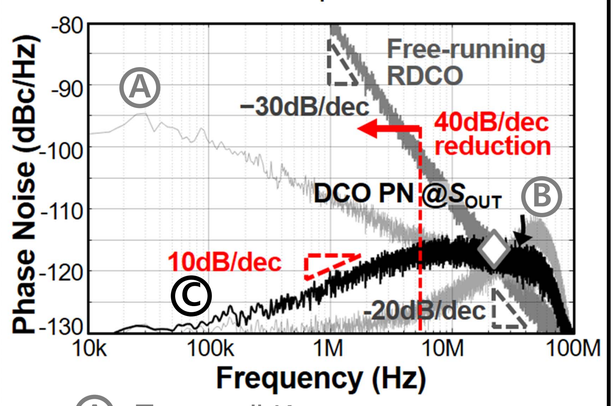
Effect of Flicker Noise



- Energy of flicker noise is concentrated at low-frequency offsets near DC
- Effect of flicker noise appears as random drifts in RDCO frequency over time
- **Flicker-induced frequency drifts (f_Ds) must be corrected through *I*-path tuning**

- f_{REF} = 125 MHz
- N = 64
- $PN_{Ring@100M}$ = −133dBc/Hz
- f_C = 20 MHz

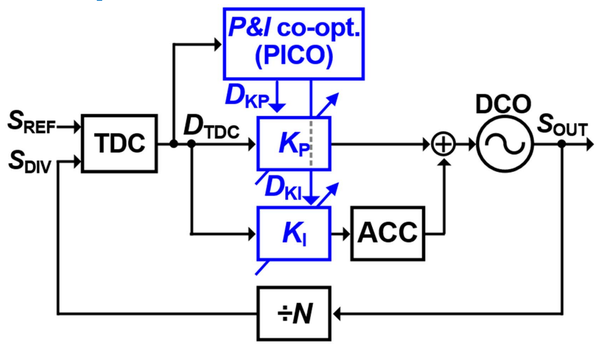


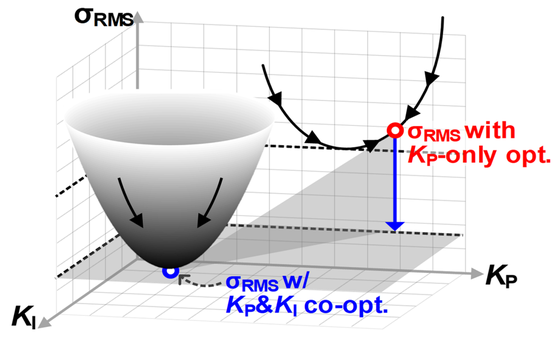


Ⓐ: Too small K_I
Ⓑ: Too large K_I
Ⓒ: Optimum K_I

Proposed *P*- & *I*-Gain Co-Optimization (PICO)

■ **Proposed Jitter Minimization Technique**





■ **Principles & Implementation of PICO**

Principles of PICO

① Cross-correlation btw $\tau_{ERR}[n]$ and $\tau_{ERR}[n+1]$ is zero
➔ $E[\tau_{ERR}[n]\cdot\tau_{ERR}[n+1]] = R\tau_{ERR}[T_{REF}] = 0$
($R\tau_{ERR}[T_{REF}]$ = autocorrelation of τ_{ERR} @T_{REF})

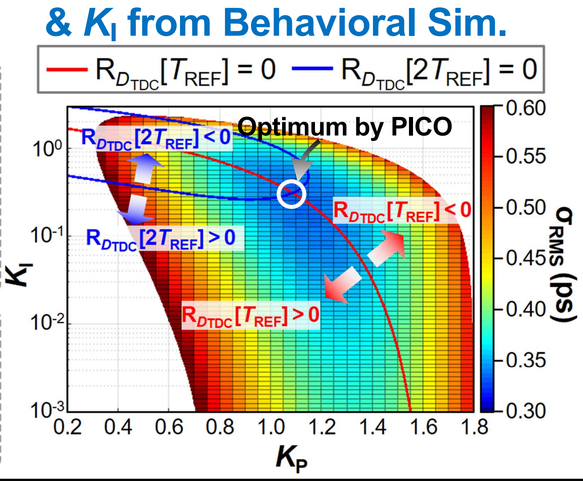
② Cross-correlation btw $\Delta f_D[n]$ and $\tau_{ERR}[n+1]$ is zero
➔ $E[\Delta f_D[n]\cdot\tau_{ERR}[n+1]]=0$, $\Delta f_D[n] \propto (\tau_{ERR}[n]-\tau_{ERR}[n-1])$
➔ $R\tau_{ERR}[T_{REF}] - R\tau_{ERR}[2T_{REF}] = 0$

Implementation of PICO

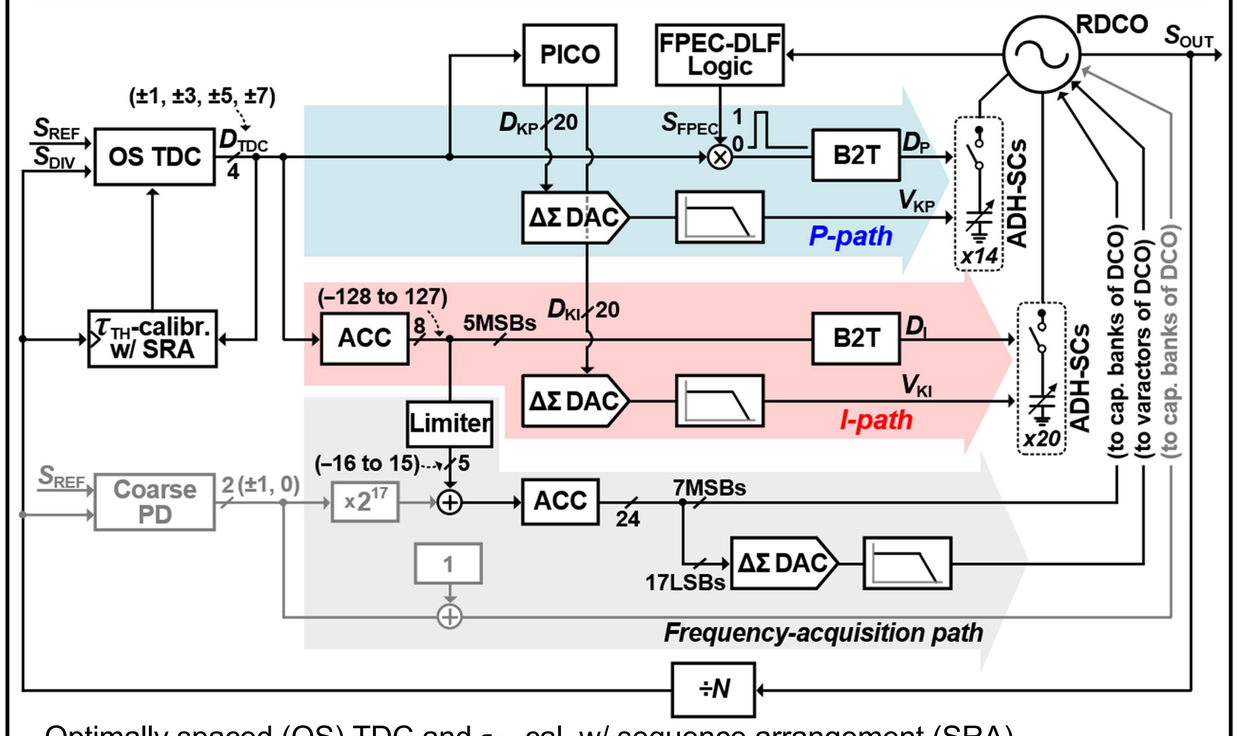
■ *P*-path: $R_{D_{TDC}}[T_{REF}] \rightarrow 0$ D_{TDC} → z^{-1} → ACC → D_{KP}

■ *I*-path: $R_{D_{TDC}}[2T_{REF}] \rightarrow 0$ D_{TDC} → z^{-2} → ACC → D_{KI}

■ **Verification: Optimal K_P & K_I from Behavioral Sim.**



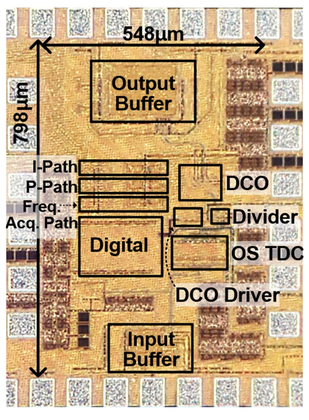
Overall Architecture

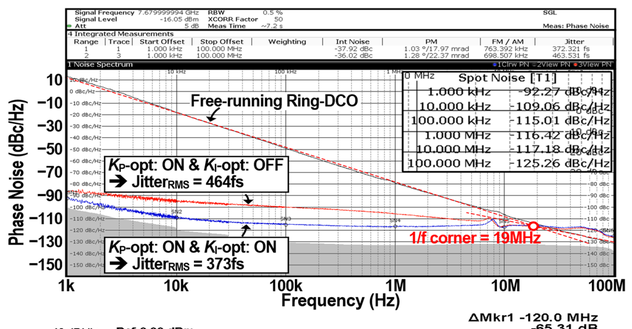


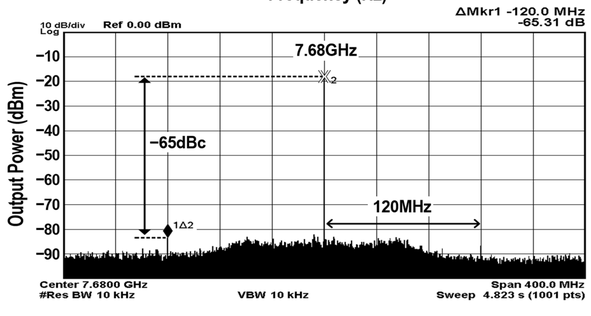
- Optimally spaced (OS) TDC and τ_{TH} cal. w/ sequence arrangement (SRA)
  ➔ High resolution & low power
- Analog-digital-hybrid switched capacitor (ADH-SC)
  ➔ precise DCO control w/ minimal loop latency
- Fast phase-error correction (FPEC) ➔ wide noise-reduction BW to lower RMS jitter

Measurement Results

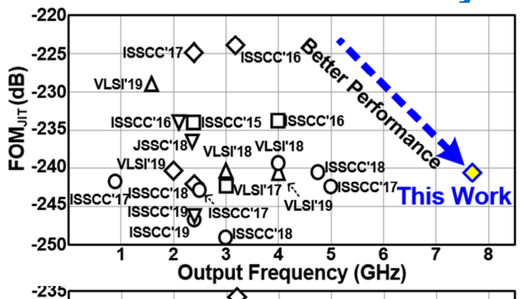
■ **Micrograph and Measurement Results**

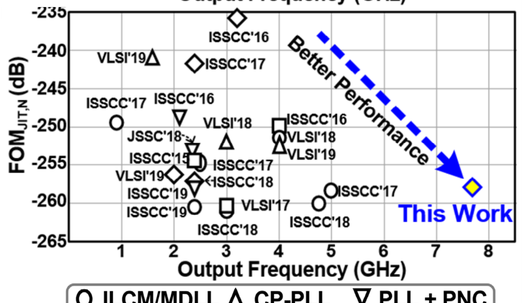






■ **Performance Summary**





○ ILCM/MDLL △ CP-PLL ▽ PLL + PNC
□ Switched-loop-filter PLL ◇ DPLL

Reference	This Work	ISSCC'19 X. Yang	ISSCC'18 T. Seong	ISSCC'18 K. M. Megawer	ISSCC'17 D. Coombs	JSSC'18 S.–S. Nagam
Architecture	DPLL	SSPLL + PNC	DPLL	ILCM	ILCM	SSPLL + PNC
Technology	65nm	28nm	65nm	65nm	65nm	65nm
Area (mm²)	0.075	0.023	0.055	0.16	0.09	0.022
f_{REF} (MHz)	120	150	75	54	125	49.15
f_{OUT} (GHz)	**7.68**	**2.4**	**2.4**	**4.752**	**5**	**2.36**
Multi. factor (N)	64	24	32	88	40	48
100kHz PN (dBc/Hz)*	**−132.7**	**−128.9**	**−124.6**	**−123.3**	**−124.0**	**−128.5**
1MHz PN (dBc/Hz)*	**−134.1**	**−133.0**	**−127.4**	**−127.2**	**−129.9**	**−126.6**
$Jitter_{RMS}$ (fs)	**373 (1k to 100M)**	**248 (10k to 100M)**	**320 (1k to 100M)**	**366 (1k to 100M)**	**340 (10k to 40M)**	**630 (1k to 100M)**
Power (mW)	6.48	4.1	6.0	6.5	5.3	5.86
FoM_{JIT} (dB)**	−240.5	−246.0	−242.1	−240.6	−242.4	−236.3
$FoM_{JIT,N}$ (dB)***	−258.5	−259.8	−257.2	−260.0	−258.4	−253.1
Spur (dBc)	−65	−63	−75	−53	−45	−55

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